

VG5000

DISK CONTROLLER

1. SCOPE

1.1 A 'devil's advocate' maximum feature / minimum component design just for VG5000.

2. FEATURES

2.1 The controller is I/O mapped as follows:

<u>PORT</u>	<u>READ</u>	<u>WRITE</u>
01	Status	Selection
00	Status Reg.	Command Reg.
20	Track Reg.	Track Reg.
40	Sector Reg.	Sector Reg.
60	Data Reg.	Data Reg.

2.2 Ports x0 address the TMS 1770. Port 01 addresses additional features:

READ: D0 Data request (1770)
D1 Command request (1770)
D2 Disk READY status
D3 Disk MOTOR status

WRITE: D0
D1 } Select 1 of 4 drives
D2 }
D3 }
D4 Double sided media (side select)
D5 Double density media *
D6 Head-load facility *
D7 ROM/RAM enable/disable

2.3 The features can be simplified by using a 6-bit cable for port 01 rather than 8. Items to omit are bits D5 and D6. Omitting other features does not give any component saving.





2.4 All drives can be daisy-chained onto a single cable.

3. COMPONENTS

3.1 The I.C. count is as follows:

1	x	TMS1770	
1	x	HN27128	
1	x	74S04	
2	x	7406	
1	x	74LS08	
1	x	74LS32	
1	x	74LS244	
1	x	74LS245	
1	x	74LS138	
1	x	74LS273 11 I.C.s.

3.2 Spare gates are as follows

74S04:	
7406:	
74LS32:	
1/2 74LS244:	(4 x )

3.3 The 244 could be used to buffer some lines:

AS	→	TMS1770
Ab	→	TMS1770
<u>RESET</u>	→	
BUSDIR	←	

3.4 Note that DRQ and INTRQ can be read via the TMS1770 status register. If no additional status is required via port 01, and no buffering is used, the 74LS244 can be omitted. In this case one further gate is freed-up:

74LS08:	
---------	---

